Please amend the claims as follows (this listing replaces all prior listings):

1. (Currently amended) A circuit comprising:

a domain-synchronizing controller ~~which produces~~ to produce a source enable signal based on a synchronous pulse signal, the source enable signal enabling ~~a source register to~~ capture of data from a source domain; and

a source-enable controller ~~which produces~~ to produce a source inhibit signal based on a relationship between a source domain clock and a destination domain clock, the source inhibit signal controlling the production of the source enable signal by the domain-synchronizing controller.

2. (Original) The circuit in claim 1, wherein the source-enable controller produces the source inhibit signal until the data is available at the source register.

3. (Currently amended) The circuit in claim 1, wherein the ~~source-enable controller produces the source inhibit signal based on~~ relationship between the source domain clock and the destination domain clock comprises a ratio between ~~a source~~ the source domain clock and ~~a destination~~ the destination domain clock.

4. (Currently amended) The circuit of claim 3, wherein the source enable controller comprises:

an event detector ~~which monitors~~ to monitor a source event signal and the source enable signal; and

a counter ~~which counts~~ to count the ratio between ~~a source~~ the source domain clock and ~~a destination~~ the destination domain clock.

5. (Original) The circuit in claim 3, wherein the source enable controller produces a source input select signal to control the selection of the data from a plurality of source registers.

6. (Currently amended) The circuit in claim 1, further comprising a destination enable controller ~~which produces~~ to produce a destination inhibit signal, the destination inhibit signal preventing the domain-synchronizing controller from producing a destination enable signal, the destination enable signal enabling a destination register to capture the data at a destination domain.

7. (Currently amended) The circuit in claim 1, wherein the domain-synchronizing controller comprises:

a plurality of flip-flops connected in a loop, the plurality of flip-flops including a first flip-flop operating ~~at a source clock frequency~~ according to the source domain clock and a second flip-flop operating ~~at a destination clock frequency~~ according to the destination domain; and

a first logic component positioned between two of the plurality of flip-flops, the first logic component inverting the output of a prior flip-flop before reaching the input of a next flip-flop to produce the synchronous-pulse signal.

8. (Original) The circuit in claim 7, wherein the source inhibit signal controls a second logic component to prevent the domain-synchronizing controller from propagating the synchronous pulse signal.

9. (Currently amended) The circuit in ~~claim 7~~ claim 8, wherein the second logic component ~~is a multiplexor~~ comprises a multiplexor.

10. (Original) The circuit in claim 8, further comprising a third logic component positioned between an input and an output for the first flip-flop, the second logic component producing the source enable signal.

11. (Original) The circuit in claim 10, further comprising a fourth logic component positioned between an input and an output for the second flip-flop, the fourth logic component producing a destination enable signal.

12. (Currently amended) The circuit in claim 10, wherein the third logic component ~~is an XOR~~ comprises an XOR gate.

13. (Original) A circuit comprising:

a plurality of flip-flops connected in a loop, the plurality of flip-flops including a first flip-flop operating on a source domain clock and a second flip-flop operating on a destination domain clock;

a first logic component positioned within the loop, the first logic component inverting the output of one of the flip-flop to produce a synchronous-pulse signal which propagates through the plurality of flip-flops; and

a second logic component receiving an inhibit signal, the second logic component preventing the propagation of the synchronous-pulse signal based on the inhibit signal.

14. (Original) The circuit in claim 13, wherein the first logic component is an inverter and the second logic component is a multiplexor.

15. (Original) The circuit in claim 13, further comprising a third logic component positioned between an input and an output to the first flip-flop, the first logic component producing a source enable signal.

16. (Currently amended) The circuit in claim 15, wherein the third logic component ~~is an XOR~~ comprises an XOR gate.

17. (Original) The circuit in claim 13, further comprising a third logic component positioned between an input and an output for the second flip-flop, the third logic component producing a destination enable signal based on the input and the output to the second flip-flop.

18. (Currently amended) A method ~~of transferring data between a source domain and a destination domain, the method~~ comprising:

producing a source-enable signal based on a synchronous-pulse signal, the source-enable signal enabling ~~a source register to~~ capture of data from a source domain; and

controlling the source-enable signal with a source-inhibit signal that is produced based on a relationship between a source domain clock and a destination domain clock, the source inhibit signal preventing ~~the synchronous pulse signal from producing~~ production of the source-enable signal until the data is available for transmission.

19. (Currently amended) The method in claim 18~~, further comprising producing the source inhibit signal based on~~ in which the relationship between the source domain clock and the destination domain clock comprises a ratio between ~~a source~~ the source domain clock and ~~a destination~~ the destination domain clock.

20. (Currently amended) The method in claim 18, further comprising producing the source-inhibit signal until the data is available at the source register or based on ~~a ratio~~ the relationship between ~~a source~~ the source domain clock and ~~a destination~~ the destination domain clock, whichever produces the source inhibit signal for a longer duration.

21. (Currently amended) The method of claim 18, further comprising:

~~monitoring a source-event signal; and~~

producing a source-input select signal which controls the selection of the data from a plurality of destination registers.

22. (Currently amended) The method in claim 18, wherein producing the source-enable signal comprises:

operating a plurality of flip-flops in a loop, the plurality of flip-flops including a first flip-flop operating ~~at a source~~ according to the source domain clock and a second flip-flop operating ~~at a destination~~ according to the destination domain clock;

inverting an output of a prior flip-flop before reaching an input of a next flip-flop to produce the synchronous-pulse signal; and

preventing a propagation of the synchronous-pulse signal through the plurality of flip-flops based on the source inhibit signal.

23. (Original) The method in claim 22, further comprising originating the synchronous pulse signal before the first flip-flop or the second flip-flop based on a selection signal.

24. (Currently amended) A circuit ~~to drive a domain register~~, comprising:

a first logic component ~~which~~ that receives a source enable signal and ~~an source~~ a source inhibit signal;

a flip-flop ~~which~~ that samples an output of the first logic component based on an inverted signal of a domain clock; and

a second logic component ~~which~~ that receives an output of the flip-flop and the domain clock, the second logic component producing a gated clock pulse to drive ~~the domain~~ a domain register.

25. (Original) The circuit in claim 24, wherein the first and second logic components are AND-gates and further comprising:

an inverter which inverts the source inhibit signal prior to being received by the first logic component.

26. (New) An apparatus comprising:

a domain synchronizing controller to produce a source enable signal based on a synchronous pulse signal, the source enable signal enabling capture of data from a source domain;

a source enable controller to produce a source inhibit signal that controls production of the source enable signal by the synchronizing controller; and

a destination enable controller to produce a destination inhibit signal that prevents the domain synchronizing controller from producing a destination enable signal that enables capture of the data at a destination domain.

27. (New) An apparatus comprising:

a domain synchronizing controller to produce a source enable signal based on a synchronous pulse signal, the source enable signal enabling capture of data from a source domain; and

a source enable controller to produce a source inhibit signal that controls production of the source enable signal by the synchronizing controller;

wherein the domain synchronizing controller comprises

flip-flops connected in a loop, the flip-flops including a first flip-flop operating at a source clock frequency and a second flip-flop operating at a destination clock frequency, and

a first logic component positioned between two of the flip-flops, the first logic component inverting the output of a prior flip-flop before reaching the input of a next flip-flop to produce the synchronous pulse signal.

28. (New) A method comprising:

producing a source-enable signal based on a synchronous-pulse signal, the source-enable signal enabling capture of data from a source domain;

producing a source-inhibit signal until the data is available at the source register or based on a relationship between a source domain clock and a destination domain clock, whichever produces the source inhibit signal for a longer duration; and

controlling the source-enable signal with the source-inhibit signal to prevent the production of the source-enable signal until the data is available for transmission.

29. (New) A method comprising:

producing a source-enable signal based on a synchronous-pulse signal, the source-enable signal enabling a source register to capture of data from a source domain;

controlling the source-enable signal with a source-inhibit signal, the source inhibit signal preventing the synchronous-pulse signal from producing production of the source-enable signal until the data is available for transmission;

monitoring a source-event signal; and

producing a source-input select signal that controls the selection of the data from destination registers.

30. (New) A method comprising:

producing a source-enable signal based on a synchronous-pulse signal, the source-enable signal enabling a source register to capture of data from a source domain; and

controlling the source-enable signal with a source-inhibit signal, the source inhibit signal preventing the synchronous-pulse signal from producing production of the source-enable signal until the data is available for transmission;

wherein producing the source-enable signal comprises

operating flip-flops in a loop, the flip-flops including a first flip-flop operating according to the source domain clock and a second flip-flop operating according to the destination domain clock,

inverting an output of a prior flip-flop before reaching an input of a next flip-flop to produce the synchronous-pulse signal, and

preventing a propagation of the synchronous-pulse signal through the flip-flops based on the source inhibit signal.